SIMD DIGITAL SIGNAL PROCESSOR AND ARITHMETIC METHOD FOR THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a Single Instruction Multiple Data (SIMD) digital signal processor and an arithmetic method for the same and particularly, to a digital signal processor for a single instruction multiple data and an arithmetic method for the same which is improved to reduce calculation amount of an algorithm having many conditional branches.

2. Description of the Background Art

Generally, a digital signal processor processes a plurality of data in the 1-cycle by applying architecture such as a Single Instruction Multiple Data (SIMD), Very Long Instruction Word (VLIW), Superscalar and the like.

Figure 1 is a block diagram showing a digital signal processor in accordance with the conventional art. As shown in the drawing, the digital signal processor includes registers 101 and 102 for storing 16-bit input data, an arithmetic unit 103 for calculating the data stored in the register according to the corresponding instruction after fetching the register and a register 104 for receiving the data calculated in the arithmetic unit 103 and storing the data.

Figure 2 is a block diagram showing a SIMD digital signal processor in

accordance with the conventional art. As shown in the drawing, the SIMD digital signal processor includes registers 201 and 202 for storing 32-bit input data, an arithmetic units 203 and 204 for calculating the data stored in the registers 201 and 202 according to the corresponding instruction after fetching the above registers and a register 205 for receiving the data calculated in the arithmetic units 203 and 204 and storing the data.

The digital signal processor with the above composition will be described as follows.

The arithmetic unit 103 calculates the data stored in the registers 101 and 102 by fetching the data when the 16-bit data is stored in the registers 101 and 102 and then stores the calculated data in the register 104. In case of a SIMD instruction data, when the each 16-bit input data is stored, each stored data is calculated in the two arithmetic units 203 and 204 simultaneously and the calculated data is stored in the register 205.

Namely, the digital signal processor shown in Figure 1 includes just an arithmetic unit 103. However, since the SIMD digital signal processor shown in Figure 2 includes two arithmetic units 203 and 204 for processing data, the digital signal processor of Figure 2 reduces the calculation time to the half of the time of the digital signal processor of Figure 1. For instance, in case of the Finite Impulse Response (FIR) filter calculation, since if the data to be processed is 256-bit and the number of the taps is 10, calculation must be repeated 256*10 times, 2560-cycle is needed. However, just 1280-cycles are necessary in case of using the SIMD digital signal processor shown in Figure 2.

However, in case of a digital signal processing algorithm having a small size of the data block to be processed and many conditional branches, there

occurs disadvantages that even if the SIMD digital signal processor shown in Figure 2 is used, calculation amount capable of being simultaneously calculated in the whole calculation is not large and it is difficult to reduce calculation time since calculation amount is not different much from that of the signal processor in accordance with the conventional art.

SUMMARY OF THE INVENTION

Therefore, the present invention provides a Single Instruction Multiple Data (SIMD) digital signal processor and an arithmetic method for the same, capable of reducing time for calculating a digital signal processing algorithm having a small size of the data block to be processed and many conditional branches

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described herein, there is provided an improved SIMD signal processor, including an on-chip program memory for storing an instruction data of a program, a plurality of main instruction decoders for outputting a decoding signal by decoding the instruction data, an on-chip data memory for storing data and a plurality of arithmetic units for calculating the data according to the decoding signal.

Also, to achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described herein, there is provided an arithmetic method for the improved SIMD signal processor, including the steps of decoding an instruction data fetched from an on-chip program memory in the main instruction decoder and calculating according to the

characteristic of the instruction data after determining the characteristic of the decoded instruction data.

The foregoing and other, features, aspects and advantages of the present invention will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

In the drawings:

Figure 1 is a block diagram showing a digital signal processor in accordance with the conventional art;

Figure 2 is a block diagram showing a SIMD digital signal processor in accordance with the conventional art;

Figure 3 is a block diagram showing an improved SIMD digital signal processor in accordance with the present invention;

Figure 4 is a data flow chart showing the data flow in case a normal instruction is calculated in Figure 3;

Figure 5 is a data flow chart showing the data flow in case a SIMD instruction is calculated in Figure 3;

Figure 6 is a data flow chart showing the data flow in case an instruction of a conditional branch is calculated in Figure 3; and

Figure 7 is a data flow chart showing the data flow after the condition is determined in Figure 3.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

Figure 3 is a block diagram showing an improved SIMD digital signal processor in accordance with the present invention. As shown in the drawing, the improved SIMD digital signal processor includes an on-chip program memory 301 for storing an instruction data for digital signal processing, a main instruction decoder 302 for decoding the instruction data by fetching the instruction data stored in the on-chip program memory 301 and outputting corresponding decoding signal, a sub instruction decoder 303 for decoding a received instruction data by fetching the instruction data stored in the on-chip program memory 301 in case of an instruction mode related to a conditional branch and outputting the corresponding decoding signal, an on-chip data memory 306 for storing the plurality of data for digital signal processing, a main arithmetic unit 304 for calculating the data according to the decoding signal of the main instruction decoder 302 and a sub arithmetic unit 305 for calculating the data identically as the main arithmetic unit 304 according to the decoding signal of the main instruction decoder 302 or calculating the data according to the decoding signal of the sub instruction decoder 303. Here, an arrow displayed with a solid line shows data flow in the normal mode and an arrow displayed with a dotted line shows data flow in the particular mode.

The digital signal processor in accordance with the present invention with above composition will be described as follows.

Firstly, the main instruction decoder 302 decodes the instruction data fetched from the on-chip program memory 301. Then, the signal processor in accordance with the present invention operates differently when the decoded instruction data corresponds to the instruction of a conditional branch or SIMD instruction or normal instruction, respectively.

First, in case of calculating a normal instruction, the decoder operates as in Figure 4. Namely, the decoded instruction data is transmitted to the main arithmetic unit 304. Then, the main arithmetic unit 304 calculates the data according to the instruction data by reading the data needed for calculation from the on-chip data memory 306 and stores the calculated data in the register (not shown) contained in the main arithmetic unit 304. At this time, the sub instruction decoder 303 and the sub arithmetic unit do not operate.

Also, in case of calculating a conditional branch, the decoder operates as in Figure 6. Namely, the decoded instruction data is transmitted to the main arithmetic unit 304. The main arithmetic unit 304 calculates data needed for calculation according to the instruction data by reading the data from the on-chip data memory 306 and stores the data in the register contained in the main arithmetic unit 304. Here, the main arithmetic unit 304 calculates the condition contained in the conditional branch. Then, the data is decoded and calculated by simultaneously fetching the instruction data to be performed in case the condition of the conditional branch is satisfied and not satisfied. Namely, the main instruction decoder 302 and the sub instruction decoder 303 respectively decode the data by simultaneously fetching the instruction data to be performed in case the condition

of the conditional branch is satisfied and not satisfied and transmit the decoded instruction data in to the main arithmetic unit 304 and sub arithmetic unit 305 independently. Then, the main arithmetic unit 304 and sub arithmetic unit 305 calculate the data needed for calculation according to the decoded instruction data by respectively reading the data from the on-chip data memory 306 and store the data in the register (not shown) contained in respective arithmetic units 304 and 305. Namely, the main arithmetic unit 304 and sub arithmetic unit 305 calculate according to the respective decoded instruction data independently.

Later, when the condition is determined, operation of the present invention is performed as in Figure 7. Namely, in case the result from the condition of the conditional branch satisfies the condition, condition of the main instruction decoder 302 and main arithmetic unit 304 is left as it is and the conditional information of the sub arithmetic unit 305 and sub instruction decode 306 is deleted. However, if the result does not satisfy the condition, the main instruction decoder 302 and the main arithmetic unit 304 delete the conventional conditional information and replace the information with the conditional information of the sub arithmetic unit 305 and sub instruction decoder 303. Then, the process after the conditional branch is continuously proceeded.

As described above, to reduce the calculation amount in processing an algorithm having many conditional branches, the present invention calculates related to a conditional branch when the conditional branch is occurred by having the main instruction decoder 302 and sub instruction decoder 303 and has the main arithmetic unit 304 and the sub arithmetic unit 305 perform independently different calculation until the condition is determined, thus to prevent instruction performance delay related with the conditional branch.

Also, the present invention can reduce the calculation time of an algorithm having many conditional branches since the present invention can prevent instruction performance delay related with the conditional branch and reduce the calculation amount.

As the present invention may be embodied in several forms without departing from the spirit or essential characteristics thereof, it should also be understood that the above-described embodiments are not limited by any of the details of the foregoing description, unless otherwise specified, but rather should be construed broadly within its spirit and scope as defined in the appended claims, and therefore all changes and modifications that fall within the metes and bounds of the claims, or equivalence of such metes and bounds are therefore intended to be embraced by the appended claims.